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Abstract

Dark current mechanisms in a 4-Transistor CMOS imager pixel with a negative gate bias on a transfer gate have been investigated. The increase of dark current with the negative gate bias has been attributed to the Gate-Induced-Leak (GIL) Trap Assisted Tunneling (TAT) by examining dark current dependency both on negative gate bias and on temperature. The negative gate bias on a transfer gate efficiently reduces Shockley-Read-Hall (SRH) dark current but generates GIL-TAT dark current when large negative gate bias is applied.

Introduction

Negative gate bias on charge transfer gate has widely been used in CCD imagers to reduce dark current generated via Si-SiO₂ interface. The mechanism of the dark current reduction with the negative gate bias was attributed to the accumulation of holes at the Si-SiO₂ interface which reduces the generation rate of dark current [1] [2]. In CMOS imager pixel, several reports have already been published regarding a negative gate bias on the 4-Transistor CMOS imager pixel transfer gate [3] [4]. The advantages of the negative gate bias are a dark current reduction and the increase of full-well capacity due to the increase of transfer gate bias swing. But it has also been reported that further lowering of negative gate bias beyond -0.9V in turn increases dark current [4]. To the author's knowledge, the mechanism of the dark current increase with negative gate bias has not been fully

understood. This paper reports the analysis of the dark current increase caused by the negative gate bias on the transfer gate, by investigating hot pixel dark signal dependency both on bias and on temperature with test pixel array AC operation.

Test Procedure

The test pixel array with 1.75 μ m pitch 2-way shared pixel was used for the dark current measurements. The pixel schematic used in the test pixel array is shown in Figure 1. The negative gate bias is applied from external power supply. The pixel raw data are taken after the on-chip Correlate Double Sampling (CDS) and Analog to Digital Converter (ADC) and are used for the analysis. Operational timing is controlled by an on-chip timing controller. Sensor chip temperature is varied by controlling the test camera atmosphere temperature. The dark image analysis is done after averaging 10 dark images so that a temporal noise in dark image can be minimized.

Experimental Results

Figure2 compares the cumulative distributions of dark signal output from test pixel array with negative gate bias of -0.9V and -1.5V. In Figure2, reduction of the number of hot pixels with a larger dark signal is observed, whereas slight increase of the number of hot pixels with a smaller dark signal is observed. This indicates that two different mechanisms for dark current generation are involved in the negative gate bias operation. Figure3 shows the reproduced dark image from the test pixel array with different

temperatures. There are two kinds of hot pixels, paired hot pixels and single hot pixel. Since the test pixel used 2-way shared architecture, dark current in paired hot pixels is likely to be accumulated in a floating diffusion. Majority of paired hot pixel dark signal has less temperature dependency than single hot pixel does. Figure4 shows activation energy distribution for hot pixel dark signals. Two negative gate bias of -0.9V and -1.5V are used in the comparison. With -0.9V gate bias majority of hot pixel has $E_a \sim 0.55\text{eV}$, which indicates SRH mechanism is the major cause of the hot pixels. With -1.5V gate bias the number of hot pixels with $E_a \sim 0.55\text{eV}$ is drastically reduced but in turn the number of hot pixels with $E_a \sim 0.2\text{V}$ increases. The results in Figure4 indicate that accumulation of holes at the Si-SiO₂ interface on the transfer gate channel is induced with the negative gate biasing and it reduces the dark current caused by SRH thermal activation mechanism. Also the results in Figure4 indicate that a different mechanism with less temperature dependency contributes to the hot pixel dark current generation and the dark current is accumulated in a floating diffusion. Figure5 shows histogram of dark signals from test pixel array. No transfer gate pulse is applied in order to see the dark current in a floating diffusion. Tail of the histogram varies with a negative gate bias, which indicates Gate Induced Leakage (GIL) is the mechanism of the dark current generation of hot pixels with large negative gate bias. The previous work of dark current analysis for 3-Transistor pixel claimed that the hot pixel dark current is caused by the GIL and the Trap Assisted Tunneling (TAT) is the key mechanism of the dark current [5]. TAT has an exponential dependency on maximum electric field [6] [7]. The TAT model can be simplified as $I_{\text{dark}} \sim A \cdot \exp[V_m/V_0]^2$, where $V_m = V_{\text{fd}} - V_{\text{gate}}$, V_{fd} is floating diffusion voltage, V_{gate} is transfer gate voltage, V_0 is field threshold voltage, and A is a proportionality factor [5] [6] [7]. Figure6 shows the hot pixel dark signal distribution dependency on V_m . V_{DD} is varied

from 2.4V to 3.0V and gate bias is varied from -0.9V to -1.5V. The combination of V_{DD} and gate bias used in the experiment is shown in Figure6(c). As shown in Figure 6(a) and (b), all the measured data seems to be scaled with V_m and the model matches with the measured data. These measured data suggest that the transfer gate negative gate bias is effective to reduce the SRH hot pixels but increases GIL-TAT hot pixels if large negative gate bias is applied.

Conclusion

The cause of dark current in 4-Transistor pixel with negative gate bias on transfer gate has been analyzed. The suppression of dark current by the ordinary SRH mechanism has been observed by applying negative gate bias. The increase of dark current beyond -0.9V negative gate bias has also been observed. The cause of the dark current increase with the negative gate bias has been attributed to the Trap-Assisted Tunneling leak current induced by Gate-bias (GIL).

References

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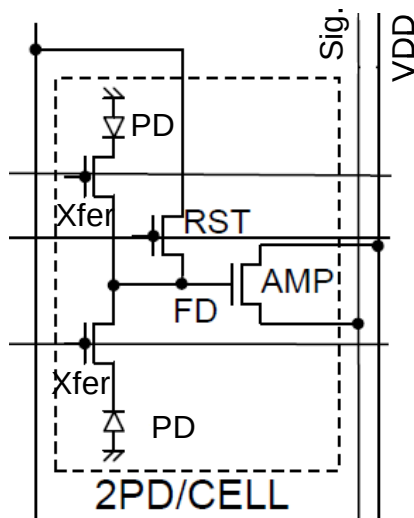


Figure1 Test pixel schematic

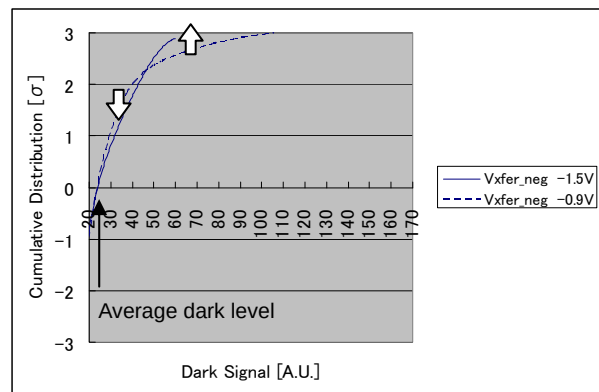
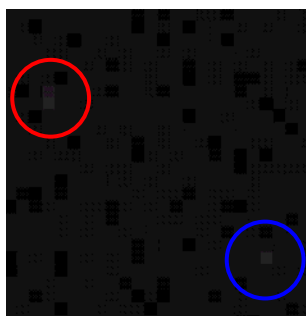


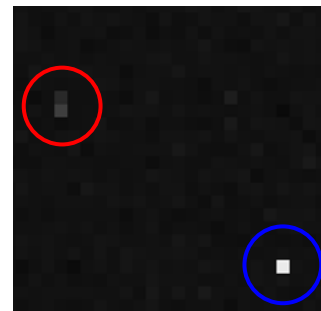
Figure2 Dark signal histogram with transfer gate negative gate bias of -0.9V and -1.5V. VDD=2.8V, 60°C.



(a) 36C



(b) 50C



(c) 80C

Figure3 Temperature dependence of hot pixels. Paired hot pixels are shown in red circle. Single hot pixel is shown in blue circle.

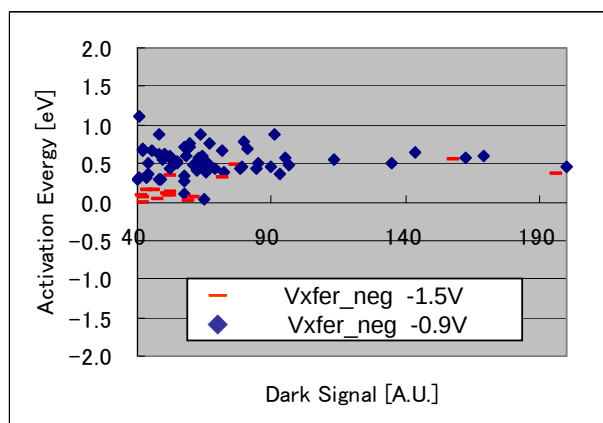


Figure4 Dark signal activation energy distribution for individual pixel.

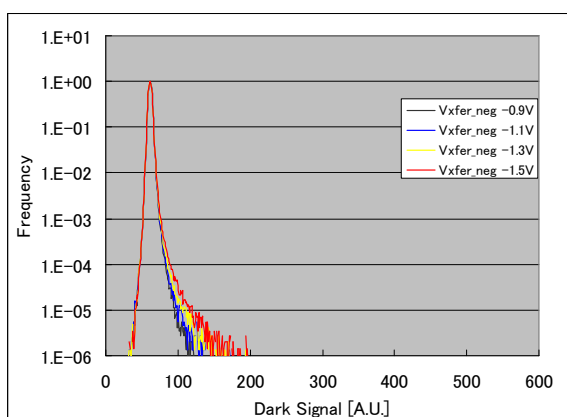
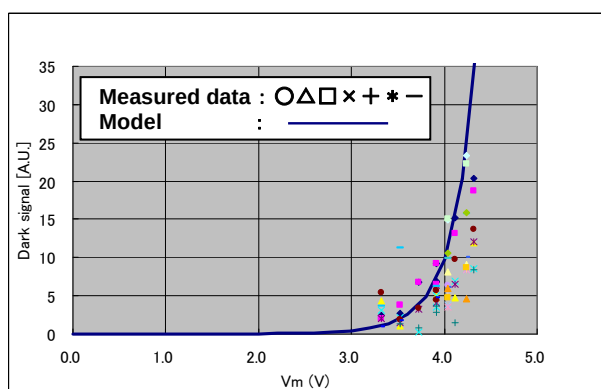
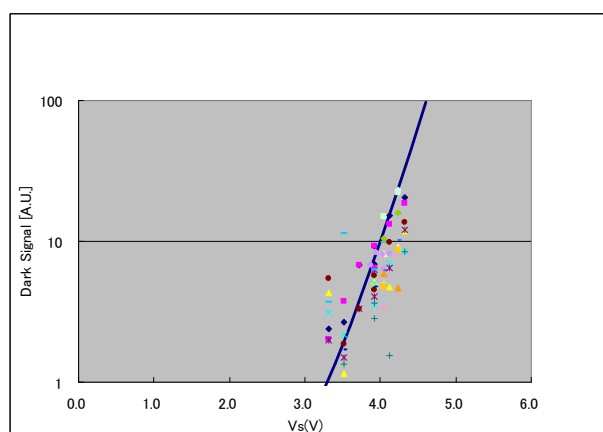


Figure5 Dark signal histogram. No transfer gate pulse is applied. VDD=2.8V, RT.



(a) Linear scale



(b) Logarithmic scale

		VDD		
		2.4V	2.8V	3.0V
Vxfer_neg	-0.9V	○	○	○
	-1.1V	○	○	○
	-1.3V	○	○	○
	-1.5V	○	○	○

(c) Biasing conditions

Figure6 Hot pixel dark signal distribution dependency on Vm. Vm is defined as Vfd – Vtransfer_neg. (a) Linear scale. (b) Logarithmic scale (c) Bias conditions used for the experiment of hot pixel dark signal distribution. RT.